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LISA K. JORGENSON
STMICROELECTRONICS, INC.
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte STUART RYAN and ANDREW JONES

Appeal 2009-003733
Application 10/621,012
Technology Center 2100

Decided: January 14, 2010

Before JAMES D. THOMAS, JOHN A. JEFFERY,
and ST. JOHN COURTENAY III, *Administrative Patent Judges*.

COURTENAY, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) (2002) from the Examiner's rejection of claims 1-6, 8, 9, 12-17, and 20-26. The Examiner indicates that claims 7, 10, 11, 18, and 19 would be allowable if rewritten in independent form. (Final Rejection 5). We have jurisdiction under 35 U.S.C. § 6(b).

We affirm in part.

STATEMENT OF THE CASE

INVENTION

The invention on appeal relates generally to prototyping of integrated systems. (Spec. 1). More particularly, Appellants' invention is directed to accessing an on-chip resource falling within the address space addressable by the processor, and accessing an interface addressable within the address space of the processor for directing packets off-chip. (Spec. 2).

ILLUSTRATIVE CLAIM

1. An integrated circuit comprising:

a processor operable to issue memory access requests, each memory access request identifying an address in memory to which the request is directed;

at least one on-chip resource falling within the address space addressable by the processor;

an interface for directing packets off-chip and addressable within the address space of the processor; and

a request directing unit for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps,

wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface, and in said second memory address map said first range of addresses are also allocated to the interface.

PRIOR ART

The Examiner relies upon the following reference as evidence:

Mitsuishi	US 6,907,514 B2	Jun. 14, 2005

THE REJECTION

The Examiner rejected claims 1-6, 8, 9, 12-17, and 20-26 under 35 U.S.C. § 102(e) as anticipated by Mitsuishi.

GROUPING OF CLAIMS

Based on Appellants' arguments in the Briefs, we will decide the appeal on the basis of claims 1, 2, 3, and 9.[1] *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUES

Appellants argue specific limitations (App. Br. 18-24) that we address *infra*. The Examiner principally contends, *inter alia*, that Appellants are arguing limitations that are not claimed. (Ans. 8). The Examiner maintains that each claimed limitation is disclosed by Mitsuishi. (Ans. 8-16). Based upon our review of the administrative record, we have determined that the following issues are dispositive in this appeal:

Issue 1: Under § 102, have Appellants shown the Examiner erred by finding that Mitsuishi discloses or describes:

[1] This decision considers only those arguments actually made. As pointed out by the Examiner (Ans. 7), Appellants have not presented arguments regarding claims 20-25. Arguments that Appellants could have made but chose not to make in the Briefs are waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

> wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface, and in said second memory address map said first range of addresses are also allocated to the interface. (Claim 1).

Issue 2: Under § 102, have Appellants shown the Examiner erred in rejecting representative claim 2 by finding that Mitsuishi discloses or describes "a mode setting pin for selectively setting a first mode in which said first address map is utilized and a second mode in which said second address map is utilized?"

Issue 3: Under § 102, have Appellants shown the Examiner erred in rejecting representative claim 3 by finding that Mitsuishi discloses or describes "wherein said request directing unit comprises switching means responsive to a mode setting signal for selectively directing the memory access request to one of said first and second address maps?"

Issue 4: Under § 102, have Appellants shown the Examiner erred in rejecting representative claim 9 by finding that Mitsuishi discloses or describes "wherein said interface comprises at least one chip-side port for transmitting memory access requests in parallel across a plurality of pins, and first and second circuit-side ports each with a reduced number of pins for communicating said packets off-chip?"

PRINCIPLES OF LAW

Anticipation under § 102

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375 (Fed. Cir. 2005) (citing *Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565 (Fed. Cir. 1992)).

> Anticipation of a patent claim requires a finding that the claim at issue 'reads on' a prior art reference. In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.

Atlas Powder Co. v. IRECO, Inc., 190 F.3d 1342, 1346 (Fed. Cir. 1999) (citations omitted).

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006). Therefore, we look to Appellants' Briefs to show error in the Examiner's proffered prima facie case.

FINDINGS OF FACT

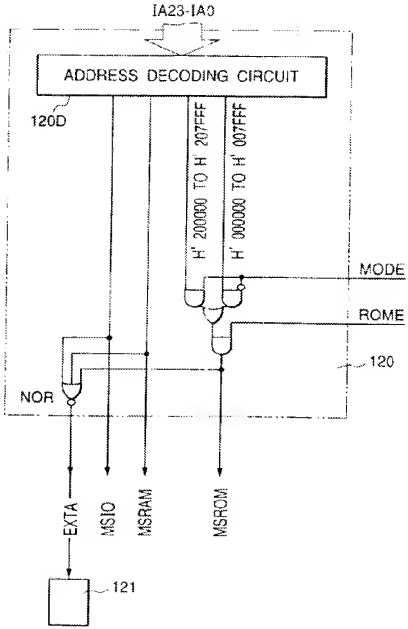
In our analysis *infra*, we rely on the following findings of fact (FF) that are supported by the record:

The Mitsuishi Reference

1. Mitsuishi discloses that "Fig. 2 is a diagram showing address maps for a predetermined operating mode of the microcomputer 1." (Col. 13, ll. 62-63).

2. Mitsuishi depicts an address decoding circuit in Figure 4 that is further controlled by MODE and ROME control signals:

FIG. 4



Mitsuishi depicts an address decoding circuit in Figure 4.

3. Mitsuishi discloses that

> ROM 5 can be mapped onto area 0 or 1 of the address map shown in FIG. 2 in dependence on the operating mode of the microcomputer 1. The ROM 5 can also be put in an unusable state by resetting a ROME signal shown in FIG. 4 at "0" through selection of a predetermined operating mode or specification of an internal I/O register.

(Col. 18, ll. 35-41).

ANALYSIS

ISSUE 1

We decide the question of whether Appellants have shown the Examiner erred in finding under § 102 that Mitsuishi discloses or describes the following limitations:

> wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface, and in said second memory address map said first range of addresses are also allocated to the interface. (Independent claims 1, 12, and 26).

At the outset, we observe that Appellants clearly present arguments for independent claims 1, 12, and 26 (argued as a group), beginning on the last paragraph of page 18 of the principal Brief.[2] We select independent claim 1 as being representative of this group.

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[2] When multiple claims subject to the same ground of rejection are argued as a group by appellant, the Board may select a single claim from the group of claims that are argued together to decide the appeal with respect to the group of claims as to the ground of rejection on the basis of the selected claim alone. Notwithstanding any other provision of this paragraph, the failure of appellant to separately argue claims which appellant has grouped

Appellants contend that (1) Mitsuishi does not show two different address maps (App. Br. 19), (2) Mitsuishi does not disclose allocating one range of addresses in an interface in a first mode and allocating another range of addresses to that same interface in a second mode (App. Br. 20), and (3), Mitsuishi does not disclose a single address range that is mapped to an on-chip resource in one mode and to an interface in a second mode. (App. Br. 21).

Regarding Appellants' first contention, we find Mitsuishi expressly discloses plural address maps: "Fig. 2 is a diagram showing address maps for a predetermined operating mode of the microcomputer 1." (FF 1, emphasis added). Therefore, contrary to Appellants' argument, we find Mitsuishi discloses at least two different address maps.

Regarding Appellants' second and third contentions, we do not reach the merits of these arguments because Appellants are arguing limitations (i.e., first and second modes) that are not recited in any of independent claims 1, 12, and 26. (App. Br. 20-21). We also note that on page 18 of the principal Brief Appellants have appended the word "only" to the claim language, as pointed out by the Examiner. (Ans. 8). Appellants additionally describe their invention in terms of the Specification at the top of page 19 of the principal Brief and conclude that "[s]uch a feature is not found in the cited reference." We note that patentability is based upon the claims. "It is the *claims* that measure the invention." *SRI Int'l v. Matsushita Elec. Corp. of America*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (*en banc*). A basic canon

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together shall constitute a waiver of any argument that the Board must consider the patentability of any grouped claim separately. *See* 37 C.F.R. § 41.37(c)(1)(vii).

of claim construction is that one may not read a limitation into a claim from the written description. *Renishaw plc v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1248 (Fed. Cir. 1998).

This reasoning is applicable here. Therefore, we find Appellants have not sustained the requisite burden on appeal in providing arguments or evidence persuasive of error in the Examiner's anticipation rejection of representative claim 1, and independent claims 12 and 26 that fall therewith.

ISSUE 2

We decide the question of whether Appellants have shown the Examiner erred in finding under § 102 that Mitsuishi discloses or describes "a mode setting pin for selectively setting a first mode in which said first address map is utilized and a second mode in which said second address map is utilized." (Representative claim 2).

Appellants contend that "[t]he 'MODE' signal in Figure 4 of *Mitsuishi* is not utilized to select one of two address maps, but is instead merely logically combined with selected address bits to selectively enable (or not enable) a particular memory device MSROM:" (App. Br. 22).

In response, we observe that there are two input control signals shown in Mitsuishi's Figure 4, a MODE control signal and a ROME control signal. (FF 2). Mitsuishi expressly discloses that

> ROM 5 can be mapped onto area 0 or 1 of the address map shown in FIG. 2 in dependence on the operating mode of the microcomputer 1. The ROM 5 can also be put in an unusable state by resetting a ROME signal shown in FIG. 4 at "0" through selection of a predetermined operating mode or specification of an internal I/O register.

(FF 3).

Therefore, we find that Mitsuishi discloses "a mode setting pin for selectively setting a first mode in which said first address map is utilized and a second mode in which said second address map is utilized" (claim 2) that occurs when "ROM 5 can be mapped onto area 0 or 1 of the address map shown in FIG. 2 in dependence on the operating mode of the microcomputer 1." (FF 3). We find that when ROM 5 is mapped to a different area (0 or 1) the address map is changed, i.e., a different or second address map results.

We also find that Mitsuishi discloses "a mode setting pin for selectively setting a first mode in which said first address map is utilized and a second mode in which said second address map is utilized" (claim 2) that occurs when "[t]he ROM 5 can also be put in an *unusable state* by resetting a ROME signal [mode setting pin] shown in FIG. 4 at "0" through selection of a predetermined operating mode . . . ." (FF 3, emphasis added). We find that placing ROM 5 in an unusable state clearly results in a different (second) address map.

Therefore, we find Appellants have not sustained the requisite burden on appeal in providing arguments or evidence persuasive of error in the Examiner's anticipation rejection of representative claim 2, and claim 13 that falls therewith. (We note that Appellants have grouped claims 2 and 13 together in the principal Brief – we have selected claim 2 as the representative claim). Claim 8 (not argued separately) falls with claim 2. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUE 3

We decide the question of whether Appellants have shown the Examiner erred in finding under § 102 that Mitsuishi discloses or describes "wherein said request directing unit comprises switching means responsive to a mode setting signal for selectively directing the memory access request to one of said first and second address maps." (Representative claim 3).

Appellants contend that Mitsuishi discloses no switching circuitry for switching between first and second address maps. (App. Br. 23).

We disagree. We affirm the Examiner's rejection of representative claim 3 for essentially the same reasons discussed *supra* regarding Issue 2. We find Mitsuishi describes a request directing unit (address decoding circuit – FF 2) that comprises switching means responsive to a mode setting signal (either the MODE or ROME signals shown in Fig. 4, FF 2) for selectively directing the memory access request to one of said first and second address maps. See our discussion of claim 2 *supra*.

Therefore, we find Appellants have not sustained the requisite burden on appeal in providing arguments or evidence persuasive of error in the Examiner's anticipation rejection of representative claim 3 and claim 14 that falls therewith. (We note that Appellants have grouped claims 3 and 14 together in the principal Brief – we have selected claim 3 as the representative claim). Claim 4 (not argued separately) falls with claim 3. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUE 4

We decide the question of whether Appellants have shown the Examiner erred in finding under § 102 that Mitsuishi discloses or describes

"wherein said interface comprises at least one chip-side port for transmitting memory access requests in parallel across a plurality of pins, and first and second circuit-side ports each with a reduced number of pins for communicating said packets off-chip." (Representative claim 9).

Appellants contend that the portion of Mitsuishi cited by the Examiner does not disclose that any of input/output ports 21-26 or 31-35 have sufficient pins for parallel transmission of memory access request packets on the chip (processor) side by having a reduced number on pins on the circuit (off-chip) side. (App. Br. 24).

The Examiner responds, as follows:

> Nothing in this claim limitation recite[s] hav[ing] sufficient pins for parallel transmission of memory access request packets on the chip (processor) side by hav[ing] a reduced number of pins on the circuit (off chip) side.
>
> In this case, Mitsuishi teaches "wherein said interface comprises at least one chip-side port for transmitting memory access requests in parallel across a plurality of pins, and first and second circuit-side ports each with a reduced number of pins for communicating said packets off-chip (e.g., fig. 1, I/O ports)." Mitsuishi teaches I/O pins (ports) for transferring data col. 11, lines 10-15. There is no teaching in Mitsuishi that an additional pin is added for doing nothing.

(Ans. 15-16).

We find the Examiner's reasoning to be unpersuasive. In particular, we find the portion of Mitsuishi relied upon in column 11 (lines 10-15) and Figure 1 provide no detail regarding the pin counts of the I/O ports. Therefore, the Examiner has not clearly established how the claimed reduced pin number limitation is expressly or inherently disclosed by Mitsuishi. Based on this record, we find that

to affirm the Examiner on this point would require speculation on our part. Because we decline to engage in speculation, we reverse the Examiner's rejection of dependent claims 9 and 17 for essentially the same reasons argued by Appellants in the Brief. (App. Br. 23-24).

CONCLUSION

Based on the findings of facts and analysis above:

Appellants have not established the Examiner erred in rejecting claims 1-6, 8, 12-16, and 20-26 under 35 U.S.C. § 102(e) as being anticipated by Mitsuishi.

Appellants have established the Examiner erred in rejecting claims 9 and 17 under 35 U.S.C. § 102(e) as being anticipated by Mitsuishi.

ORDER

We affirm the Examiner's rejection of claims 1-6, 8, 12-16, and 20-26 under 35 U.S.C. § 102(e).

We reverse the Examiner's rejection of claims 9 and 17 under 35 U.S.C. § 102(e).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

rwk

LISA K. JORGENSON
STMICROELECTRONICS, INC.
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006